

## REMARKS

Claims 1-7 are pending in the application. The Examiner has objected to Figure 11. A Replacement Figure accompanies this amendment, with the appropriate designation of Figure 11 as "Prior Art". The Examiner has objected to the Specification due to an informality on page 16. Applicants submit herein an amendment to the Specification that corrects that informality without adding new matter. The Examiner has rejected Claim 7 under 35 USC 101 as non-statutory subject matter. By this amendment, Applicants have amended the language of Claim 7 in accordance with the Examiner's suggestion. Claims 1, 6 and 7 have been rejected under 35 USC 103(a) as being unpatentable over Settle in view of Tsubouchi; Claim 2 has been rejected as unpatentable over Settle in view of Tsubouchi and further in view of Mendenhall; and Claims 3-5 have been rejected as unpatentable over Settle, Tsubouchi, Mendenhall and further in view of Yamauchi. For the reasons set forth below, Applicants believe that the claims are patentable over the cited art.

The present invention provides a format conversion circuit comprising a memory for storing video data; a header generation device for generating a packet header

that adheres to a standard for motion picture compression; a synchronous timing detector for detecting a synchronizing signal for the video data; and a selection device for repeating the selection of the packet header generated by said header generation means and selection of a predetermined amount of video data read out of said memory as a payload responsive to the packet header, during an interval from when said synchronous timing detection device detects the synchronizing signal until it detects the next synchronizing signal. The format conversion method and program storage device are additionally taught and claimed.

The Settle patent provides teachings regarding generating a packet header. The Examiner has acknowledged that Settle does not disclose the storing of unpackitized data in a memory, the detecting of a synchronizing signal, or the selection of a predetermined amount of video data read out of the memory as a payload responsive to the packet header during an interval between synchronizing signals. The Examiner has cited the Tsubouchi patent as providing the teachings which are missing from the Settle patent.

The Tsubouchi reference teaches that it is known to store video in a buffer and to read the video data out of the buffer in response to a signal. Tsubouchi does not,

however, teach or suggest selection of a predetermined amount of video data as a payload of a generated packet header in response to detection of a synchronizing signal during an interval between detection of successive synchronizing signals.

Applicants respectfully assert that the Federal Circuit has stated that when patentability turns on the question of obviousness, the obviousness determination "must be based on objective evidence of record" and that "this precedent has been reinforced in myriad decisions, and cannot be dispensed with." (In re Lee, 277 F. 3d 1338, 1343 (Fed. Cir. 2002)). Moreover, the Federal Circuit has stated that "conclusory statements" by an examiner fail to adequately address the factual question of motivation, which is material to patentability and cannot be resolved "on subjective belief and unknown authority" (Id. at 1343-1344). Applicants respectfully assert that neither Settle nor Tsubouchi teaches or suggests the claim feature of selection of a predetermined amount of video data during an interval between successively detected synchronizing signals. While Tsubouchi teaches releasing video in response to a signal, Tsubouchi does not teach or suggest releasing a predetermined amount of video during an interval between successive synchronizing signals.

Further, there is nothing in the teachings of either Settle or Tsubouchi to motivate one having skill in the art to modify Settle with a video buffer of Tsubouchi. Further, even if one were to modify Settle with a video buffer, one would not arrive at the subject invention since neither reference teaches or suggests the detection of successive synchronizing signals and the selection of a predetermined amount of video data between the detected signals.

For a determination of obviousness, the prior art must teach or suggest all of the claim limitations. "All words in a claim must be considered in judging the patentability of that claim against the prior art" (*In re Wilson*, 424 F. 2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970)). Since the cited references fail to teach each and every one of the claim limitations, a *prima facie* case of obviousness has not been established by the Examiner against Claims 1, 6 and 7.

Applicants respectfully assert that the Examiner has also failed to establish a *prima facie* case of obviousness against the remaining claims. The primary reference against all claims is Settle. Applicants rely on the arguments set forth above with respect to the teachings of Settle, alone and in combination with the Tsubouchi reference. Applicants further assert that the additionally

cited references do not provide the teachings which are missing from the combination of Settle and Tsubouchi. Mendenhall is cited for its teaching of a counter that counts packet header size. Applicants respectfully assert that Claim 2 recites a counter that counts the amount of packet header output as well as the amount of video data read out of memory, in combination with the feature of Claim 1 and the claimed switch. Clearly the addition of the Mendenhall packet header counter is not sufficient to obviate the invention as claimed.

The additionally-cited Yamauchi patent is cited for its teaching of producing a clock signal locked to the horizontal synchronization signal included in video input. The Examiner states that "it was known to sample video based on a horizontal synchronization signal". Applicants respectfully assert that, even if one were motivated to use a horizontal synchronization signal to sample video from the Settle system with a Tsubouchi video buffer, one would not arrive at the claimed invention since none of the references teaches or suggests the detection of successive synchronizing signals and the selection of a predetermined amount of video data between the detected signals (Claim 3), with the counter counting and outputting a data valid signal (Claim 4) and a FIFO memory being reset in response

to a data valid signal (Claim 5). Further, none of the cited references teaches erasing stored video data, as is expressly recited in Claim 5.

Based on the foregoing amendments and remarks, Applicants respectfully request entry of the amendment, reconsideration of the rejections, and issuance of the claims.

Respectfully submitted,  
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